Synopsys' PrimeTime Advanced Low Power Signoff Technology

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ABSTRACT

Join this session to learn more about technologies that help designers during timing closure and signoff for low power designs.

Designs built to operate at wider voltage ranges take advantage of both high-performance and low-power characteristics of FinFET technology. This can create a challenge for library management and signoff timing coverage.

Synopsys will share the latest innovations in Voltage Scaling that relieves the requirement of characterizing and handling libraries at every operating voltage and variation level, significantly reducing design cost, margining, and turnaround time.

TSMC and Synopsys will share results and user experience from the latest 7nm early design starts.

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Synopsys' PrimeTime Advanced Low Power Signoff Technology

TSMC Open Innovation Platform Ecosystem Forum

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Outline

Low Power Methodology Trends

Impact of Low Power Methodologies

Library Scaling Methodology

Summary

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Low Power Methodology Trends

- **Low Voltage**
  - Lower voltage operation is one of the most effective ways to reduce power
- **Dynamic Voltage and Frequency Tuning**
  - Recent designs use multiple power domains to independently control supply voltage
    - Stand-by Frequency/Voltage
    - Nominal Frequency/Voltage
    - High-performance Frequency/Voltage
    - Near continuous frequency tuning
- **Simultaneous Multi-Voltage Analysis**
  - Independent power domains have different supply regulators
    - Per block/module application
    - Different drift/variation, etc.

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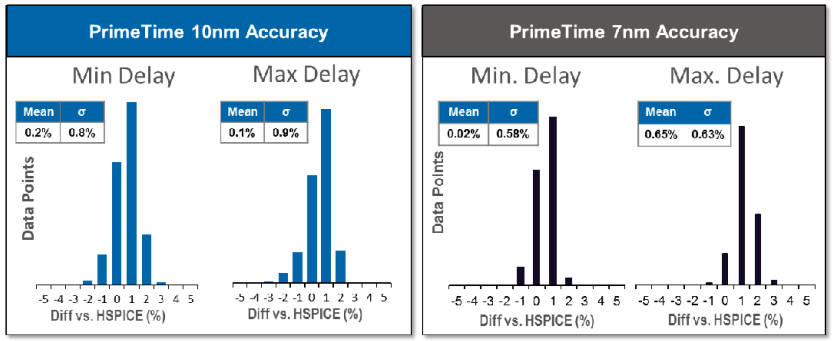
Impact of Low Power Methodologies

Low Voltage Golden Accuracy using Advanced Waveform Propagation

- AWP continues to deliver great spice correlation
- 30+ Customer Logos signing off with PrimeTime at FinFET nodes



Source: Synopsys Customer Data

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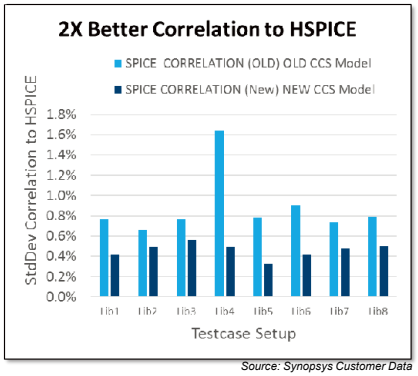
LTAB Submission: June 2016

Impact of Low Power Methodologies

Golden Accuracy is getting better: Liberty CCS Enhancements

- **Improvements for 10/7-nm support**
  - Support for improved CCS receiver model with multiple segments
  - Support for per-grid CCS noise model
- **Overall improvement in accuracy vs. HSPICE**



Source: Synopsys Customer Data

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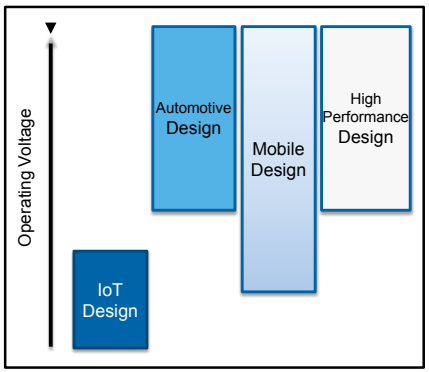
Impact of Low Power Methodologies

Library Needs: Versatile Operating Voltage

- **7nm FinFET transistors can operate at wide voltage ranges**
  - More frequency and voltage modes achievable (DVFS)
- **Timing library characterization completed early in design flow**
  - Additions/ Changes can result in costly late re-characterization
- **Signoff accurate timing results at range of voltage applications with a static set of libraries**
  - Library Scaling



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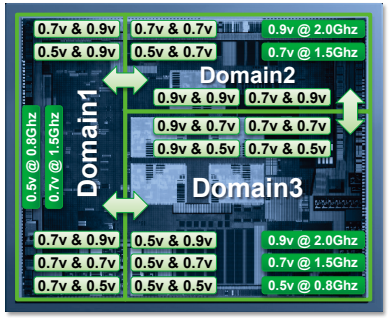
Impact of Low Power Methodologies

STA Needs: Efficient Multi-Voltage DVFS Analysis

- Timing signoff needs to be done at many speed and voltage combinations
- Simultaneous multi-voltage analysis significantly reduces the quantity of runs required
- Signoff accurate timing results at required voltages with dynamically varying frequencies



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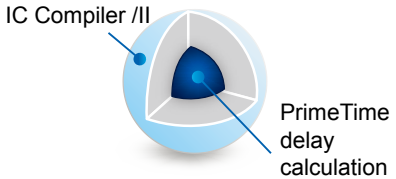
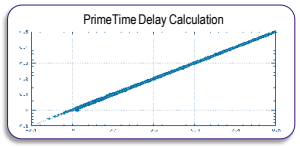
Efficient Timing Closure: Signoff Delay Calculation inside Place& Route





PrimeTime to IC Compiler II Slack Correlation

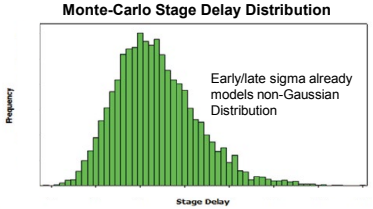
- **PrimeTime Delay Calculation inside IC Compiler /II**
  - Delay calculation is the inner kernel of static timing analysis. Computes delays and slews for a single primitive, e.g. stage delay.
  - Support for advanced STA technologies including Advanced Waveform Propagation (AWP) and Parametric On-Chip-Variation (POCV)

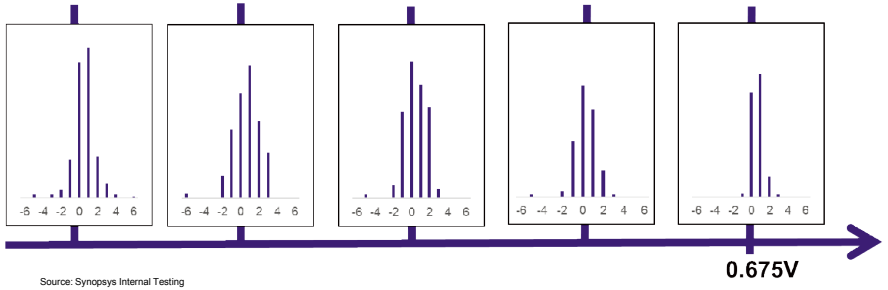
Source: Synopsys Internal Testing

Impact of Low Power Methodologies

Variation: Low Voltage Accuracy using POCV

- Great POCV accuracy at today's low voltages



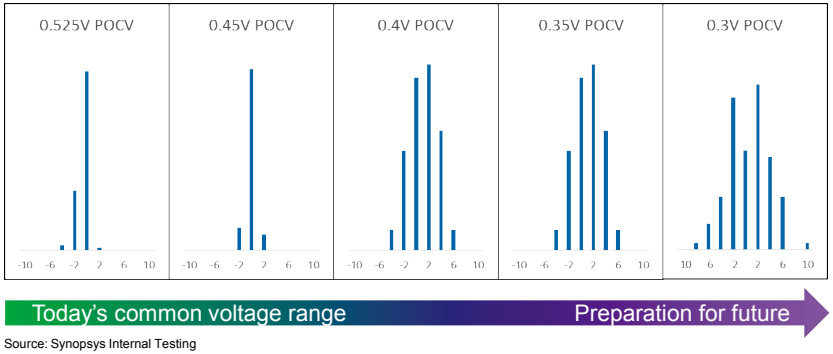


Source: Synopsys Internal Testing

Impact of Low Power Methodologies

Variation: Ultra-Low Voltage POCV Correlation

- **Variation increases drastically with Ultra-low Voltage**
  - TSMC and Synopsys are exploring possible extensions to LVF

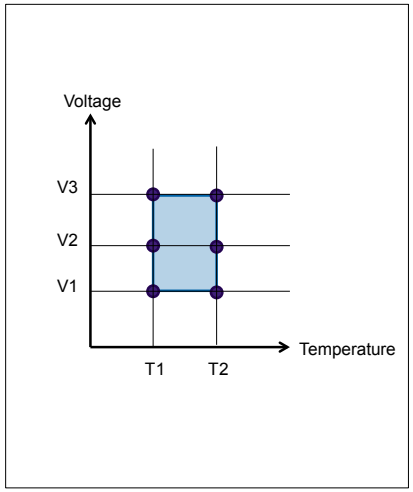


Source: Synopsys Internal Testing

Library Scaling Methodology

Introduction to Library Voltage Scaling

- Scaling is interpolation of library data characterized at a specific operating condition to an intermediate operating condition applied to the design
- Reduces # of libraries needed



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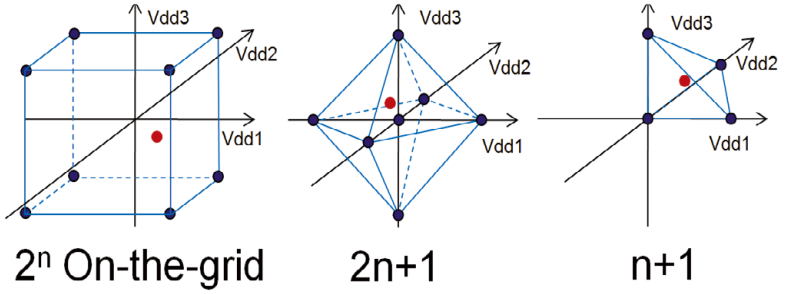
Library Formations for Scaling Group

- PrimeTime supports three library formations



2^n On-the-grid 2n+1 n+1

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Library Scaling Eco-system

	Library Compiler	PrimeTime	Documentation Training
Library Requirements	N/A	N/A	✓
Recommended Flow	N/A	N/A	✓
Library Checks	Primary	Secondary	✓
Library Formation Checks	✓	✓	✓
Operating Condition (Library usage Checks)	N/A	✓	✓

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Assessing Library Scaling Accuracy

- **Good Scaling Accuracy Starts with Good Libraries**
- **Accuracy of library scaling is important in the design context**
  - Measure scaled calculation accuracy on design paths w.r.t. SPICE
- **SPICE accuracy for library scaling is checked in the same way as non-scaled corner SPICE accuracy**

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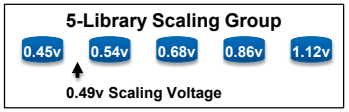
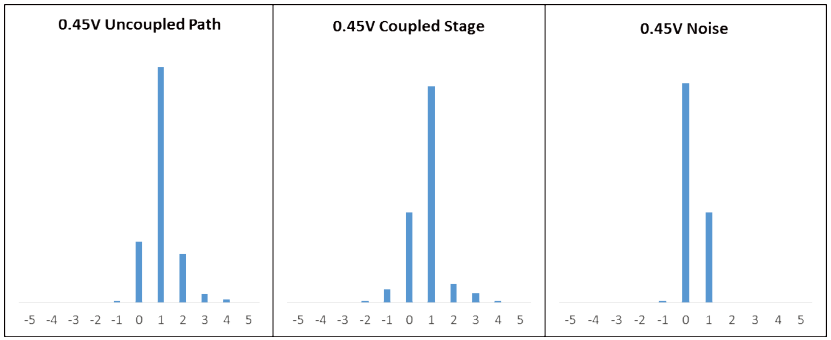
Good Scaling Accuracy Starts with Good Libraries

Library Accuracy at Characterization Corner compared to SPICE

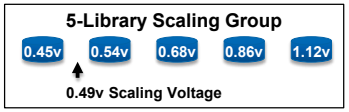


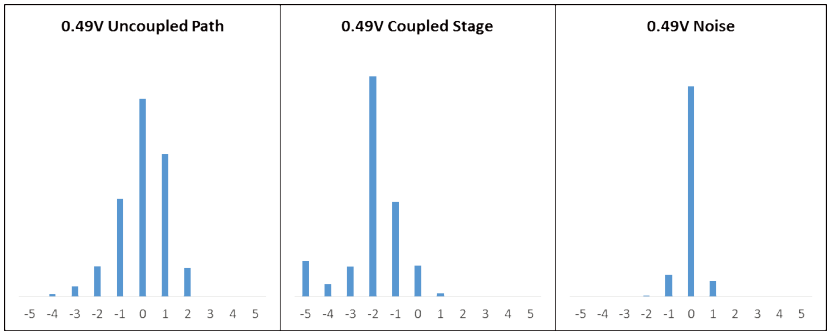


Source: Synopsys Internal Testing

Scaling Accuracy

Library Accuracy at Scaled Voltage compared to SPICE

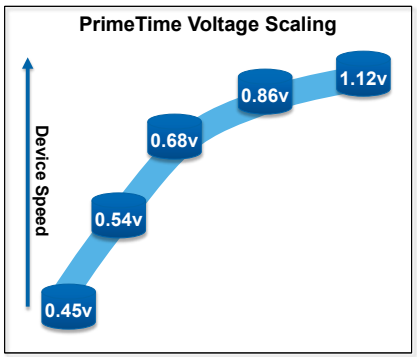




Source: Synopsys Internal Testing

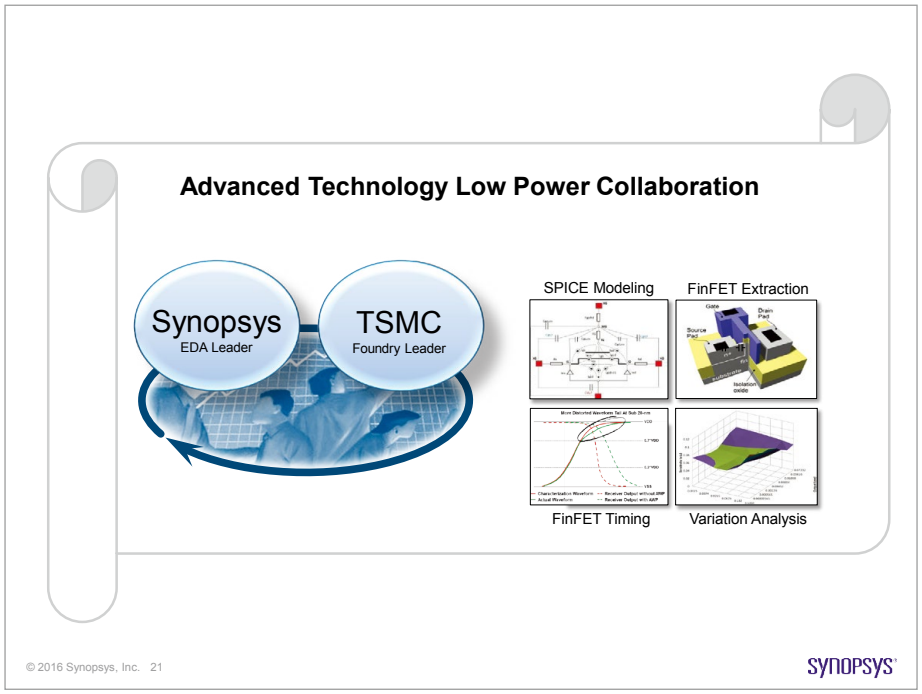
Signoff Accurate Voltage Scaling

- **Accurate scaling methodology is available today**
- **5 libraries enable scaling over the entire operating range for most designs**
- **No extra margin needed for scaling methodology**



Summary

- **7nm FinFET transistors can operate at very wide voltage ranges**
  - More frequency and voltage modes achievable for low power designs
- **Timing signoff needed at many speed and voltage combinations**
  - Dictates signoff results at any voltage with fixed set of libraries
- **Low Power Methodologies have significant impact on tools/flows**
- **PrimeTime provides good support on low voltage accuracy, scaling library needs, variation and timing closure**
- **TSMC and Synopsys are continuously collaborating on**
  - Base Calculation Accuracy
  - Variation
  - Scaling Libraries


Advanced Technology Low Power Collaboration
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EDA Leader
TSMC
Foundry Leader
SPICE Modeling
FinFET Extraction
FinFET Timing
Variation Analysis
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